REMARKS

Attached herewith is a Request for Continued Examination of the present application. The appropriate fees are included.

**I. Specification**

The specification is objected to under 37 CFR 1.75(d)(1) as failing to provide proper antecedent basis for claims 32 "changing a width of the first FET" in claim 32, and "making the first channel wider."

As best understood by the Applicant, the Examiner believes that making variations in the width of the channel is not supported, which is an objection that was previously made. However, as addressed in the previous Response, the Applicant's respectfully argued that the objection is incorrect. Applicant refers the Examiner to the chart on page 11, which illustrates that the gate widths and lengths may be adjusted as desired. For instance, the channel width of FET M5 in the hardened circuit of FIG. 6 appears to have been significantly altered as compared to the corresponding FET M5 for the prior art circuit in FIG. 1. Please note that the specific example of FIG. 6 is intended only as an example of a presently preferred embodiment of the invention. Please note further that M5, M6, M7, and M8 act in coordination with each other and that the example discusses only the occurrence of a glitch at node 134 which node is clearly part of a feedback loop circuit configuration. Moreover, to attempt to show all possible variations of the present invention is impractical. Instead, Applicant provides more than sufficient information

and examples of use of the invention so that one of skill in the art can apply the invention to any particular type of component of interest.

If the Examiner disagrees with the above and provides more specificity in his objection, then perhaps Applicant will be able to discern what changes would resolve the issue.

**II. Claim Rejections – 35 USC §112**

Claim 11 (and Claims 12-13 via Dependency)

The Applicant notes with appreciation the §112 issues pointed out by the Examiner relative to Claim 11. Claim 11 is amended in a manner believed to remove the 35 USC §112 rejection made to claims 11-13.

Claim 30

The Examiner states that Claim 30 is misdescriptive of the elected embodiments. The Applicant respectfully traverses this rejection. The Examiner states that there is only one logic gate illustrated in FIG. 6, for example, e.g. item 612, and that the claim calls for one or more logic gates. However, the Applicant respectfully argues that the Examiner's understanding that FIG. 6 illustrates only one logic gate is incorrect. To support the Applicant's argument, the Applicant points the Examiner to FIG. 6, which clearly illustrates a pair of inverters, items 612 and 613. It is commonly known in the art that an "inverter" is either a (1) logical function that returns the opposite of the input and equivalent to a NOT gate or (2) a device that changes direct current into alternating current (i.e., a power converter). It is commonly known in the art that an inverter as defined by a logical function that returns the opposite of the input and equivalent to a

NOT gate is a type of logic gate. The Applicant respectfully argues that the specification clearly defines the inverter as a logical function that returns the opposite of the input (and not a power converter). For example, on page 14, line 3, it is stated:

> "When the signal applied to ClB (Clear bar) is low, the output of inverter 1008 is high which turns on FET 1010 and drives the Q node low."

Further areas in the specification that include the same description can be found on page 2, line 17. The pair of inverters 612 and 613, illustrated in FIG. 6, corresponds to the prior art circuit shown in FIG. 1, which includes the pair of inverters 128 and 130 (see page 2, line 4). In further support of Applicant's argument that one or more logic gates are clearly illustrated in FIG. 6, the Applicant argues in order to harden the circuit, two embedded delays 606 and 608 are added to the prior art circuit of FIG. 1 to form the circuit of FIG. 6. (see p. 10, line 28- p 11, line 3). As stated in the specification on page 4, line 1, a delay may comprise an inverter, which as described above, is a type of logic gate. Therefore, there is clearly more than one logic gate illustrated in FIG. 6. And hence, Claim 30 is exactly descriptive of the elected embodiments. The Applicant respectfully traverses this particular rejection and requests reconsideration in light of the arguments made herein.

As per the Examiner's comments, Applicant has corrected the lack of antecedent basis by changing "circuits" to "elements." The Applicant notes with appreciation this §112 issue as pointed out by the Examiner.

As per the Examiner's comments, Applicant has replaced "subsequent logic element" with the earlier used wording to increase clarity and to eliminate the lack of antecedent basis. The Applicant notes with appreciation this §112 issue as pointed out by the Examiner.

As per the Examiner's comments, Applicant has replaced "subsequent logic device" with the earlier used working to increase clarity and eliminate the lack of antecedent basis. The Applicant notes with appreciation this §112 issue as pointed out by the Examiner.

Applicant has made appropriate claim amendments as suggested by the Examiner in conjunction with additional claim amendments that are believed to remove the outstanding objections to the claims.

Claim 31 (and Claims 32-37 via Dependency)

Applicant has amended claim 31 to remove the ambiguous reference to "providing" as indicated by the Examiner. The Applicant notes with appreciation this §112 issue as pointed out by the Examiner.

The Examiner also states that the recitation of "adjusting the characteristics of the first channel of the first FET" appears to be misdescriptive because the specification only discloses adjusting the FETs of the embedded delay. The Applicant respectfully traverses this rejection. However, Applicant respectfully argues that the Examiner's statement is incorrect. The specification provides extensive discussion on the fact that the original circuit to be hardened, i.e., the circuit of FIG. 1, may be modified extensively so as to form the circuit of FIG. 6. See for instance, p. 10, line 30 where the specification discusses a modified portion 604. For even more detail into the changes made between the circuit of FIG. 1 and FIG. 6, Applicant suggests the Examiner evaluate the chart on page 11 wherein extensive changes are made in the width and length of the FET channels. The Examiner is also encouraged to evaluate the circuits, which include a statement of the width and length for the FETs in the non-hardened and hardened

circuits. The Applicant respectfully traverses this particular rejection and requests reconsideration in light of the arguments made herein.

Accordingly, the amendments to claim 30 and 31 are believed to remove the rejection under 35 USC §112 to dependent claims 31-37.

**III. Claim Rejections – 35 USC §102**

Claims 8 and 10 stand rejected under 35 U.S.C. 102(b) as being anticipated by Bansal (USPN 5,504,703), referred hereinafter as **Bansal**. Claims 30 and 37 are not specifically rejected but, as best understood from the discussion, the Examiner also intended to reject these claims under 35 U.S.C. 102(b).

A rejection under 35 U.S.C. §102 must contain every element recited in the claim in as complete detail as is contained in the claim and arranged as recited in the claim. MPEP §2131 provides:

> A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. *Verdegall Bros. v. Union Oil Co. Of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the . . . claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim.

The Applicant respectfully argues that because from the facts derived from the reference, as set forth below, the cited reference does not contain every element recited in the rejected claims in as complete detail as is contained in the claims and arranged as recited in the claims. Thus, the

rejection is unsupported by the art and should be withdrawn.

First, Claim 8 stands rejected because, as best understood, the primary claimed feature at issue is:

> ". . . the input to output pulse response of the logic gate and the two or more logic elements being substantially similar in that the resulting amount of pulse propagation delay and amount of reduction of the pulse width of the potentially producing SEU producing glitch is spread substantially evenly among the logic gate and the two or more logic elements. (ref: Claim 8 of Applicant's application) (emphasis added)

**Bansal** does not specifically state whether or not his designed delays are different (or spread equally) as between the logic gate and the inverters in the feedback path as per the previous claim language. Applicant agrees with the Examiner that **Bansal** does not expressly disclose the claimed feature at issue. Therefore, according to the MPEP as quoted above, **Bansal** must *inherently describe* the claimed feature at issue *in as complete detail* as contained in the claim. The Examiner argues that **Bansal** does inherently describe the claimed feature in as complete detail as contained in the claimed feature because 1) ever logic element must have a delay and 2) **Bansal** does not expressly state that his delays are different, thus, his delays must be the same. (ref: December 17, 2004 Office Action, page 5, lines 3-7 and page 6, lines 9-16) The Applicant respectfully argues that the Examiner's logic on this matter is overly simplistic, flawed, and ignores the fundamental anticipation rules as required by the MPEP for the following reasons. First, the Examiner is assuming that all logic gates have the same delay (because, according to the Examiner, if the delays are not expressly different, they must be the same). This is a false assumption. It is commonly known in the art that logic elements have a unique delay that is adjustable via a variety of factors. In fact, if two unrelated logic elements were provided at

random and their delays were unknown, it would be more probable than not that the two logic elements would have different delays. Second, the Examiner's logic can be just as easily reversed. Specifically, the argument would be: **Bansal** doesn't expressly state that his delays are the same, thus, his delays must be different. The foregoing argument has as much weight and credibility (if not more weight and credibility due to the argument made *infra*) as the Examiner's argument. Third, the Applicant's specification describes in detail the technical reasoning behind the claimed feature at issue (ref: page 11, line 4 through page 13, line 6 with particular attention to page 12, lines 3-15). No such information, suggestion, or motivation is contained in **Bansal**. There is no technical nexus in **Bansal** that would lend one of ordinary skill in the art to conclude that **Bansal** inherently describes the claimed feature at issue. And there is certainly no technical nexus to conclude that **Bansal** describes the claimed feature in as complete detail as contained in the claim. Fourth, the Applicant argues that **Bansal**'s specification lends one to believe that his inverters have unique (and thus, different) delays. Specifically, **Bansal** provides a preferred embodiment of his inverter in '703, FIG. 4. **Bansal** also states (multiple times) that the channel width and length of transistors Tp and Tn are selected to provide a *desired* delay (specific to each inverter because of **Bansal**'s reference to FIG. 4, which is a preferred embodiment of an inverter). (ref: '702, Col. 3, lines 34-36 and Col. 4, lines 6-8) If **Bansal** intended the delaying action to be the same for each inverter, why expressly state that the channel width and length of the transistors are selectable, per inverter, to provide a desired delay? Why not just state the width and length are standard and not configurable? It is apparent that **Bansal** desires maximum flexibility in the delay time combinations for his inverters and thus, infers different delays for each inverter. After all, **Bansal** is more concerned with the total delay time of an inverter pair

(ref: '703, Abstract, lines 2 and 5; Col. 2, lines 56-57; Col. 3, lines 29-31; Col. 3, lines 53-54; Col. 4, line 1; Col. 4, lines 49-51; Col. 6, lines 9-11). And thus, it is logical to infer that **Bansal** desires maximum design flexibility by combining different delay times for each inverter in a pair and a different delay time for each pair of inverters. It appears that the Examiner's entire argument is that **Bansal** might possibly use the claimed feature, because **Bansal** never states anything about it one way or the other. Applicant respectfully submits that the mere possibility that Applicant's invention might be used in **Bansal** does not form the basis for a 102 rejection. For instance, if a first invention is a camera and a second invention is a special lens, the mere possibility that the special lens might be used in camera does not mean the camera anticipates the special lens. Likewise, the mere possibility that **Bansal** might use Applicant's claimed features, if he knew what they were, does not mean that **Bansal** anticipates. Simply stated, contrary to the Examiner's statement that all elements are disclosed in the **Bansal** reference, the claimed feature at issue is not (either expressly or inherently described in as complete detail as in the claim), so according to the MPEP, the rejection is unsupported by the art and must be withdrawn.

Second, Claim 10 stands rejected based on similar logic the Examiner uses relative to Claim 8. Specifically, the Examiner argues that since **Bansal** doesn't expressly state that the rise time and fall time of each inverter is different, then the rise time and fall time must be the same. First, the Applicant makes the same arguments as in the previous paragraph. In sum, since **Bansal** doesn't expressly state the claimed feature at issue, the MPEP requires that **Bansal** must inherently describe the claimed feature at issue in as complete detail as in the claimed feature. Simply stated, the Examiner argues that **Bansal** inherently describes the claimed feature at issue in as complete detail as the claimed feature because **Bansal** doesn't expressly state the claimed

feature at issue. Obviously, this type of logic is greatly flawed and violates the fundamental anticipation rules as required by the MPEP. Second, the Applicant notes that the Examiner's argument relative to rise and fall time is slightly different to his argument relative to delay time for the following reasons. With regards to delay time, **Bansal** actually teaches a delay time. With respect to rise time and fall time, **Bansal** doesn't even mention rise time or fall time. A word search of **Bansal** for "rise" and "fall" resulted in no matches. Thus, the Examiner's argument is essentially: **Bansal** doesn't suggest or teach a rise time and fall time (at all), therefore, the rise time and fall time must be the same. Again, this type of logic is full of flaws and certainly not supported by the MPEP. Third, although rise time and fall time are related to the overall delay, these parameters are certainly not synonymous. It is commonly known in the art that delay time is the time delay between an input signal and the corresponding output signal. Semiconductor manufacturers specify it as the time delay from the leading edge of the input signal, which assumes negligible rise/fall time, to the 50% point of the comparator-output rise/fall time. A delay is related to the rise/fall time, but rise times for two different circuits may be different and if the fall times are approximately the same, then the circuits may have a similar delay because the circuit delay will be most correlated to the fall time. Thus, two logic gates having the same or similar delay time doesn't necessarily equate to the rise/fall times being balanced. **Bansal** notes that there is parasitic and interconnective capacitance (ref: '703, Col. 3, lines 27-35). These characteristics could very possibly affect the rise and fall times. Again, the Examiner's entire argument is that **Bansal** might possibly also disclose the claimed feature at issue in Claim 10 because **Bansal** never states anything about it one way or another. The Applicant respectfully traverses this rejection. The rejection is unsupported in the art and must

be withdrawn.

Third, although not clear from the Office Action, the Examiner may be arguing that Claims 30 and 37 are inherently described by **Bansal**. Again, as responded to the Examiner's previous arguments above, this argument presupposes numerous limitations discussed in great detail by the Applicant, but not mentioned by **Bansal**. In short, a technical nexus, taught or suggested in **Bansal**, to bridge the gap between **Bansal** and the Applicant's application is not provided by the Examiner. In addition, there is no reason to believe that the **Bansal** circuit is even likely to provide that the input to output responses to L1 and L2 are approximately equal for the logic elements and logic gates. In fact, this seems unlikely. "Inherent anticipation requires that the missing descriptive material is 'necessarily present,' not merely probably or possibly present, in the prior art." *Trintec Industries v Top-USA Corp.*, 295 F.3d 1292, 1295, (Fed. Cir. 2002). Therefore, it is insufficient that the missing limitations "may be" in the prior art; the missing limitation "must" in fact be there. In fact, without Applicant's specific teachings, one of skill in the art would not know how to build Applicant's circuit from the **Bansal** disclosure. Because the Examiner admits that **Bansal** plainly does not contain every element in as complete detail as is contained in amended Claims 30 and 37, and because **Bansal** plainly does not place the claimed matter in possession of the public, Applicant respectfully submits that the rejection to amended Claims 8 and 30, and their dependent claims, is accordingly traversed.

The Examiner states that **Bansal** does not show the claimed features of Applicant's device, but then argues that the features might be included in **Bansal**. The Examiner has failed to establish a *prima facie* case because **Bansal** is completely inadequate to be enabling or

anticipating. How would one of skill in the art know what to do by examining **Bansal** without any teaching *or suggestion* to do so? To anticipate, the identical invention must be shown or inherently described with as complete detail as in the rejected claim. In short, the Examiner's arguments lack the requisite technical "missing link," which must be taught or suggested by **Bansal**, to bridge the gap between **Bansal** and the Applicant's claims.

With all due respect, the Examiner has clearly failed to establish a *prima facie* case under 35 U.S.C. §102. It is respectfully submitted that a rejection under 35 U.S.C. §102 must contain every element recited in the claim in as complete detail as is contained in the claim and arranged as recited in the claim. M.P.E.P. § 2131. "The identical invention must be shown in as complete detail as is contained in the claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir "1989) See also M.P.E.P. (Manual of Patent Examining Procedure) § 2131. Further, "[A]nticipation requires that ... the prior art reference must be enabling, thus placing the alleged disclosed matter in the possession of the public." *Akzon v. U.S. Int'l Trade Commission*, 808 F.2d 1471, 1 USPQ 2d 1241, 1245 (Fed. Cir. 1986) (citing *In re Brown*, 329 F.2d 1006, 1011, 141 USPQ 245, 249 (C.C.P.A. 1964) (emphasis added).

Because the Examiner admits that **Bansal** plainly does not contain every element in as complete detail as is contained in amended claims 8, 10, 30 and 37, and because **Bansal** plainly does not place the claimed matter in possession of the public, Applicant respectfully submits that the rejection to amended claims 8 and 30, and their dependent claims, is accordingly traversed.

Any additional amendments made were not necessary to overcome the cited prior art.

## IV. Conclusion

It is submitted in view of these remarks that all grounds for rejection have been removed by the foregoing amendments and discussion. Reconsideration and allowance of this application are therefore earnestly solicited.

The Examiner is invited to phone Mr. Theodore Ro, attorney for Applicant, 281-244-7148, if in his opinion such a phone call would serve to expedite the prosecution of subject patent application.

Respectfully submitted,

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